ABSTRACT

A flash memory controller is disclosed. The flash memory controller includes a processor for executing at least one operation and arbitration logic coupled to the processor. Data from the arbitration logic allows the processor to perform the at least one operation for a flash memory device. In one aspect of the present invention, the processor utilizes data from the arbitration logic to direct a search for available blocks to the particular flash memory device. In another aspect of the present invention, the processor utilizes an internal buffer within the flash memory device to store valid data during the search before the valid data is relocated. As a result, the search time for available blocks is greatly shortened and the need for an external buffer is eliminated. Consequently, the speed at which block management operations are performed is significantly increased.